Amendm nts to th Claims

Claims 1-21 (Canceled).

22. (Currently Amended): The circuitry of ~~claim 21~~ claim 25 wherein the capacitor dielectric region consists essentially of dielectric aluminum nitride.

23. (Currently Amended): ~~The circuitry of claim 21~~ DRAM circuitry comprising:

an array of word lines forming gates of field effect transistors and an array of bit lines, individual field effect transistors comprising a pair of source/drain regions; and

a plurality of memory cell storage capacitors associated with the field effect transistors, individual storage capacitors comprising a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode, a capacitor dielectric region received intermediate and contacting each of the first and second capacitor electrodes, the capacitor dielectric region having a thickness less than or equal to 60 Angstroms and comprising dielectric aluminum nitride, the other of the pair of source/drain regions of the one field effect transistor being in electrical connection with one of the bit lines; and

wherein the capacitor dielectric region consists essentially of dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

Claim 24 (Canceled).

25. (Currently Amended): ~~The circuitry of claim 21 wherein~~ DRAM circuitry comprising:

an array of word lines forming gates of field effect transistors and an array of bit lines, individual field effect transistors comprising a pair of source/drain regions; and

a plurality of memory cell storage capacitors associated with the field effect transistors, individual storage capacitors comprising a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode, a capacitor dielectric region received intermediate and contacting each of the first and second capacitor electrodes, the capacitor dielectric region ~~has~~ having a thickness less than ~~or equal to~~ 50 Angstroms and comprising dielectric aluminum nitride, the other of the pair of source/drain regions of the one field effect transistor being in electrical connection with one of the bit lines.

Claims 26 and 27 (Canceled).

28. (Currently Amended): ~~The circuitry of claim 21~~ DRAM circuitry comprising:

an array of word lines forming gates of field effect transistors and an array of bit lines, individual field effect transistors comprising a pair of source/drain regions; and

a plurality of memory cell storage capacitors associated with the field effect transistors, individual storage capacitors comprising a first capacitor electrode in electrical connection with one of a pair of source/drain regions of one of the field effect transistors and a second capacitor electrode, a capacitor dielectric region received intermediate and contacting each of the first and second capacitor electrodes, the capacitor dielectric region having a thickness less than or equal to 60 Angstroms and comprising dielectric aluminum nitride, the other of the pair of source/drain regions of the one field effect transistor being in electrical connection with one of the bit lines; and

wherein the dielectric aluminum nitride is substantially amorphous.

Claims 29-64 (Canceled).

65. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region consists essentially of substantially amorphous dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes.

Claim 66 (Canceled).

67. (Previously Presented): The circuitry of claim 28 wherein the capacitor dielectric region has a thickness less than or equal to 50 Angstroms.

68. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region consists essentially of substantially amorphous dielectric aluminum nitride.

Claim 69 (Canceled).

70. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region consists essentially of substantially amorphous dielectric aluminum nitride, and has a thickness less than or equal to 50 Angstroms.

71. (Currently Amended): The circuitry of claim 28 wherein the capacitor dielectric region consists essentially of substantially amorphous dielectric aluminum nitride and native oxide formed on at least one of the first and second capacitor electrodes, and has a thickness less than or equal to 50 Angstroms.

Claims 72 and 73 (Canceled).

74. (Currently Amended): The circuitry of ~~claim 21~~ claim 23 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.

75. (Previously Presented): The circuitry of claim 28 wherein the bit lines are received elevationally outward of the memory cell storage capacitors.

76. (New): The circuitry of claim 23 wherein the capacitor dielectric region has a thickness less than 50 Angstroms

77. (New): The circuitry of claim 28 wherein the capacitor dielectric region has a thickness less than 50 Angstroms.